

;16U2 VECTOR SCOPE
;TAPE RECORDER

TFH8: BUS INPUT CHANNELS?
;CH ADDRESS ;CH DATA OUT

;BUFFERED
BUS OUTPUTS

;DEBUGGING POINTS

;CONTROLS

NC 16U2-00
E1A-OUT 16U2-01
E1A-IN 16U2-02
HIGH-E1A 16U2-03
HIGH-E1A 16U2-04
HIGH-E1A 16U2-05
HIGH-E1A 16U2-06
GND 16U2-07
NC 16U2-08
NC 16U2-09
NC 16U2-10
CLEAR-PC 16U2-11
CLEAR 16U2-12
NC 16U2-13
NC 16U2-14
NC 16U2-15
NC 16U2-16
NC 16U2-17

V12-PLUS 16U2-00
V12-MINUS 16U2-01
BRIGHT 16U2-02
X-SCOPE 16U2-03
V12-PLUS 16U2-04
V12-MINUS 16U2-05
Y-SCOPE 16U2-06
NC 16U2-07
NC 16U2-08
NC 16U2-09
NC 16U2-10
NC 16U2-11
NC 16U2-12
NC 16U2-13
T-CLO-IN 16U2-14
T-CLO-OUT 16U2-15
TAP-OUT 16U2-16
NC 16U2-17

16U1-00 NLOCK-OUT 16U1-00 CLEAR
16U1-01 READ-27 16U1-01
16U1-02 WRITE-27 16U1-02
16U1-03 FROM-18 16U1-03
16U1-04 FROM-11 16U1-04
16U1-05 POP 16U1-05
16U1-06 RC 16U1-06
16U1-07 PUSH 16U1-07
16U1-08 RET 16U1-08
16U1-09 AA-1 16U1-09
16U1-10 AA-2 16U1-10
16U1-11 INT-0 16U1-11
16U1-12 INT-1 16U1-12
16U1-13 INT-2 16U1-13
16U1-14 INT-3 16U1-14
16U1-15 INT-68800 16U1-15
16U1-16 NC 16U1-16

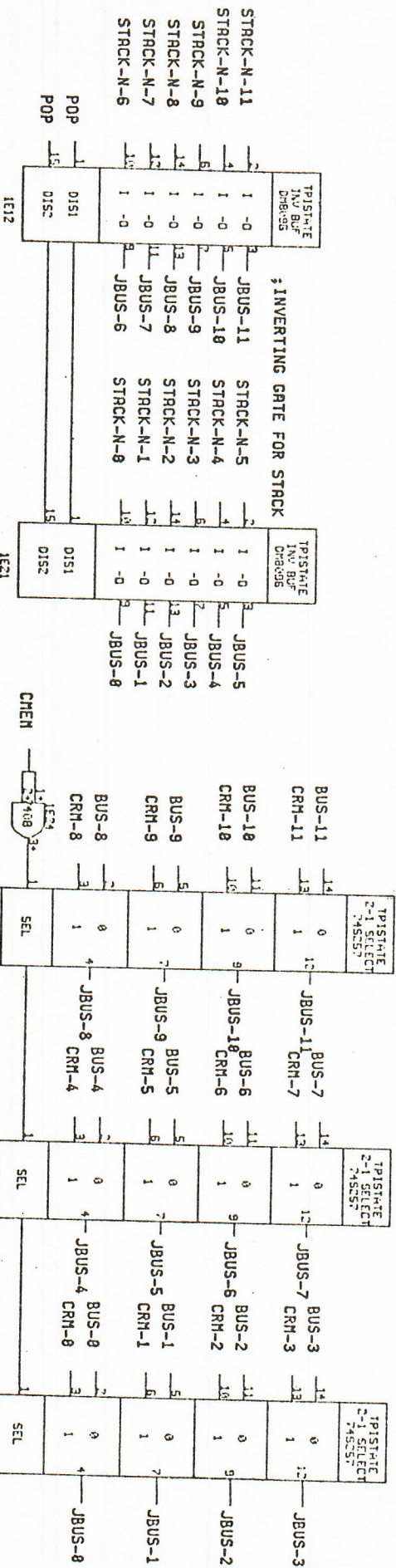
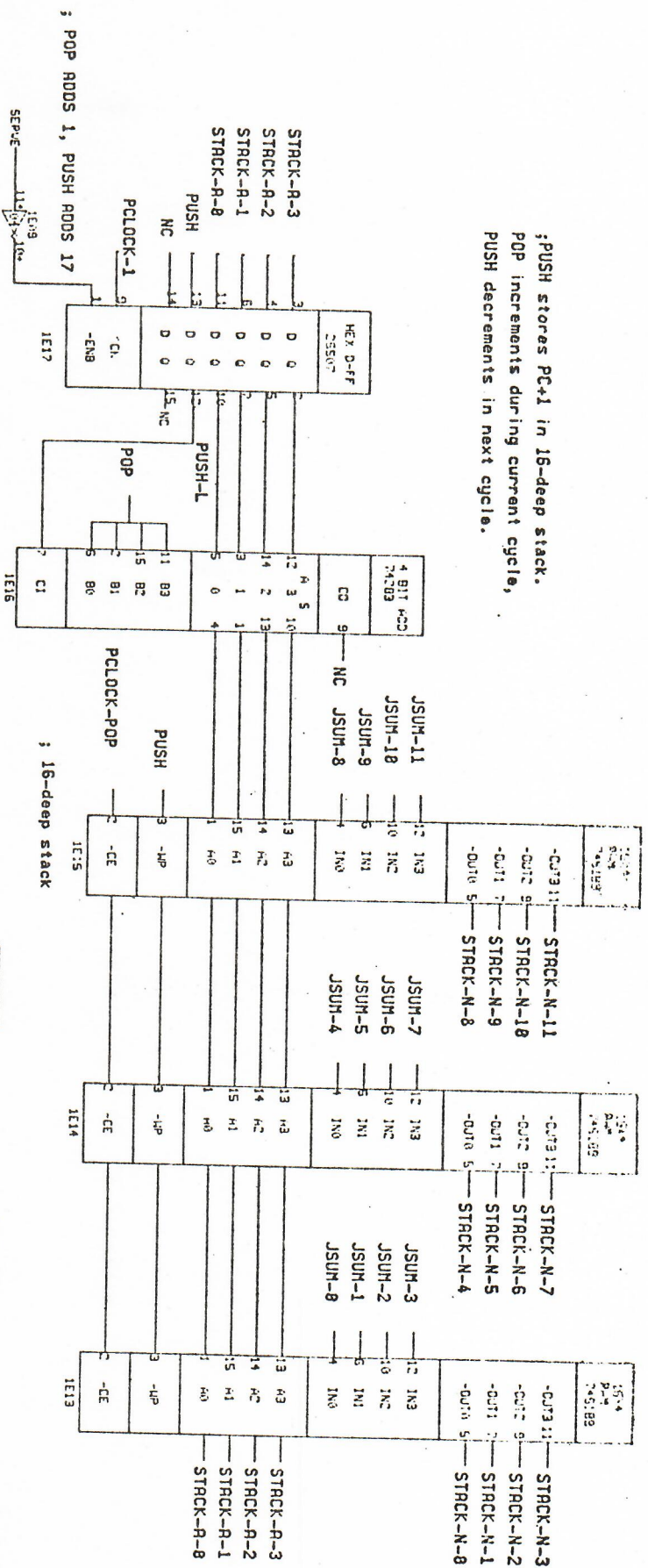
68-HZ-CLOCK 16U1-00
POWER-ON 16U1-01
BATT-5-N 16U1-02
BATT-5-N 16U1-03
BATT-5 16U1-04
BATT-5 16U1-05
TIMER 16U1-06
PWR-DN 16U1-07
NC 16U1-08
NC 16U1-09
BATT-12 16U1-10
BATT-12 16U1-11
BATT-12-N 16U1-12
BATT-12-N 16U1-13
NC 16U1-14
V12-MINUS 16U1-15
V12-MINUS 16U1-16
;POWER CONNECTOR

MR-0 16U1-00
MR-1 16U1-01
MR-2 16U1-02
MR-3 16U1-03
MR-4 16U1-04
MR-5 16U1-05
MR-6 16U1-06
MR-7 16U1-07
MR-8 16U1-08
MR-9 16U1-09
MR-10 16U1-10
MR-11 16U1-11
MR-12 16U1-12
MR-13 16U1-13
MR-14 16U1-14
MR-15 16U1-15

16U2-00 VCC 16U2-00 BUSWRITE
16U2-01 V12-MINUS 16U2-01 BUSREAD
16U2-02 KB-PARITY 16U2-02 BB-8
16U2-03 KB-STROBE 16U2-03 BB-1
16U2-04 KB-0 16U2-04 BB-2
16U2-05 KB-OENB-H 16U2-05 BB-3
16U2-06 KB-1 16U2-06 BB-4
16U2-07 KB-SH-H 16U2-07 BB-5
16U2-08 KB-2 16U2-08
16U2-09 KB-CTRL 16U2-09
16U2-10 KB-3 16U2-10
16U2-11 KB-4 16U2-11
16U2-12 KB-5 16U2-12
16U2-13 KB-RESET 16U2-13
16U2-14 KB-6 16U2-14
16U2-15 KB-7 16U2-15
16U2-16 KB-ERROR 16U2-16
16U2-17 NC 16U2-17

;KEYBOARD

; PUSH stores PC+1 in 16-deep stack.
 POP increments during current cycle,
 PUSH decrements in next cycle.



;SERVE forces STRACK-N to 111 111 111 111 for
 interrupt servicing; i.e., to address 8

;JBUS is tri-state PC-address bus. POP attaches stack. JMP-LOW attaches crm
 for jumps. CMEN attaches BUS for crm-loading. Default is JSUM (page 9).

STACK TO PC GATE

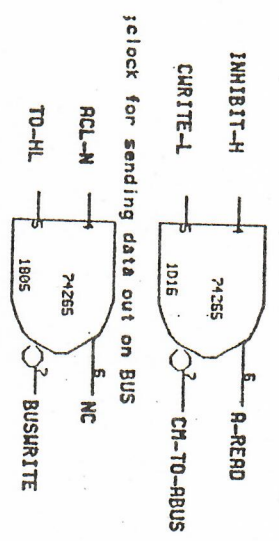
STACK

05-APR-76 14:20

HQM: NTFH1

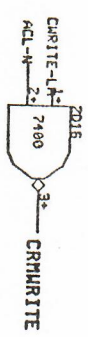


1E22



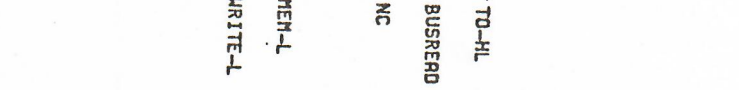
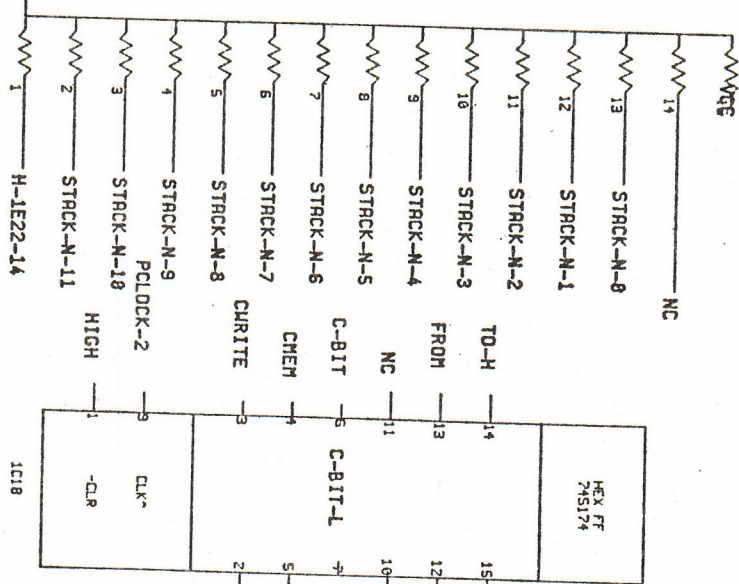
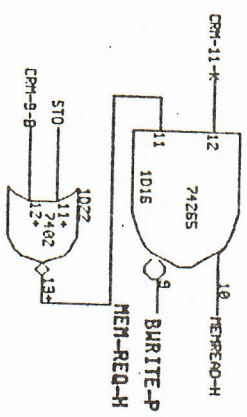
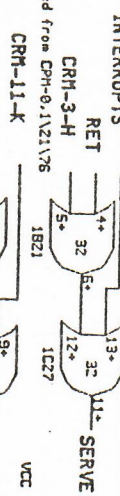
;clock for sending data out on BUS

;write clock loads CRH



NTFH2 2016 MUST BE 74 S 00
;inhibit pop during POPJ1
priority interrupt

;and jump to 8



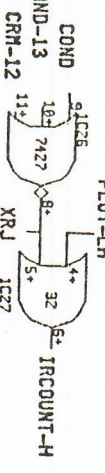
;if CRH-9 is 1 in an operate-class instruction (8 8xx x1), it is a 32-bit 2-cycle command. The INHIBIT signal disables the instruction decoder in cycle 2 and connects CRH output to the A-BUS. A = OP(+1,B). EXCEPTION: during CURITE, normal arithmetic is done and the result goes into CRH data input

;CHEN orders use "RESULT" of last instruction for CRH address, using automatic "push-pop" to remember the location during the inhibited cycle. CURITE gets data from BUS in second cycle.

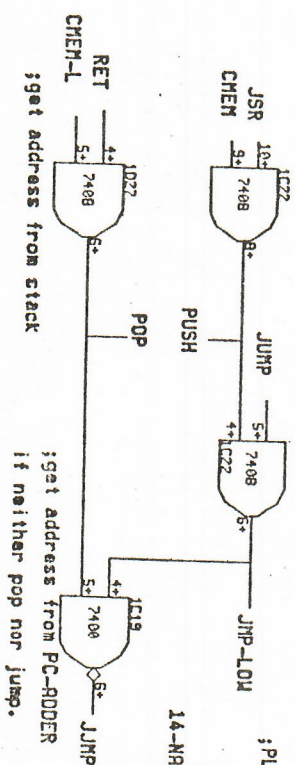
; READ A B WRITE A B
M(R) ==> B B ==> M(R)
and OP(R,B) ==> R
828 888 824 888
INC 822 848 826 848
DEC 820 828 824 828

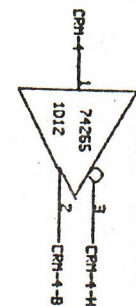
CREAD A B CURITE A B
821 888 825 888
OP(C(RESULT),B) ==> R
OP(R,B) ==> C(RESULT)
and also ==> R

;PLOT increments XR for vector length
PLOT-LH



COND 14-NAND-13
CRH-12
;XRj increments XR in auto-iterate cond





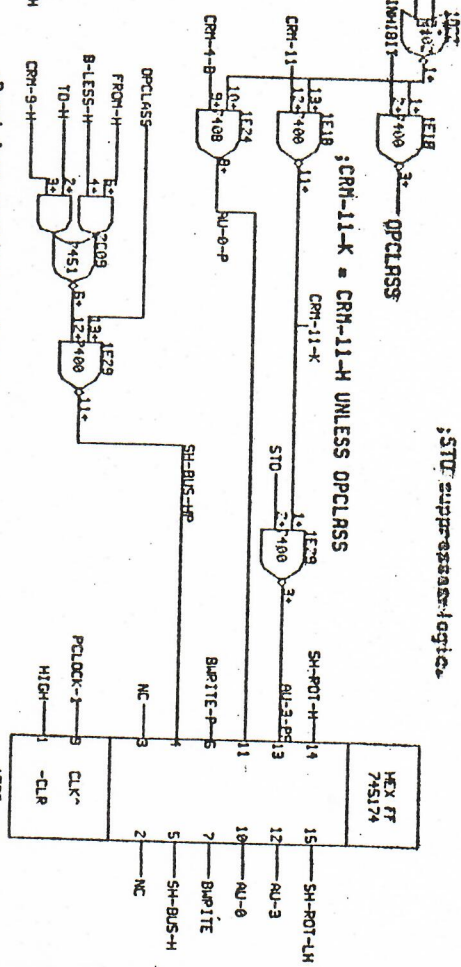
1808 is ROTATE, suppressed during memory cycles.

ROT is 0110, suppressed by ST0

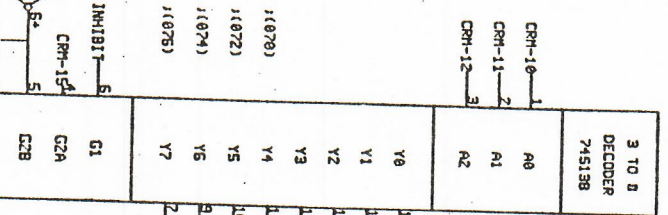
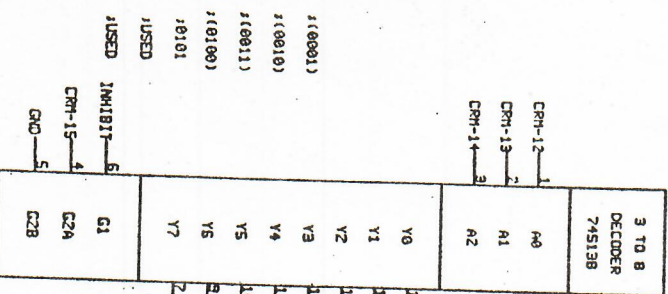
Read from working register.

ST0 suppresses logic

READ-READY-RESET STRETCHED FOR TWO CYCLES

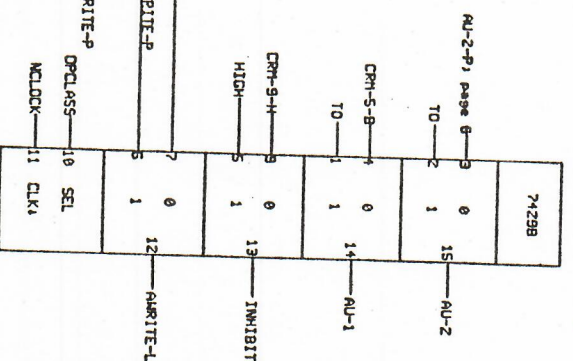


THE CODES FOR THE ALU ARE LATCHED FROM
RU-3 RU-2 RU-1 RU-0
TO 0-0-0-0
FROM 0-1-1-0
SH-ROT-H 1-0-0-0
SH-CRM-H 0-1-1-0 IS CHANGED TO 0-0-1-0

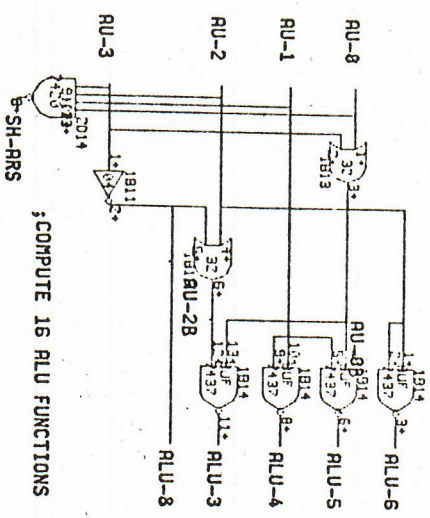


NOP; NO RWRITE
OPIF C-BIT

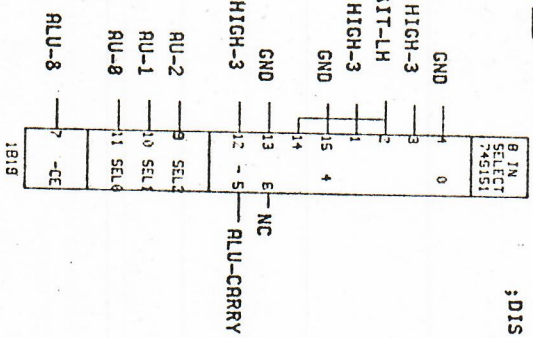
RWRITE after OPCLASS except when suppressed by NOP or OPIF-and-C-BIT. ALSO, RWRITE WITH GET <10, B.



; OP IS 1111



; COMPUTE 16 ALU FUNCTIONS



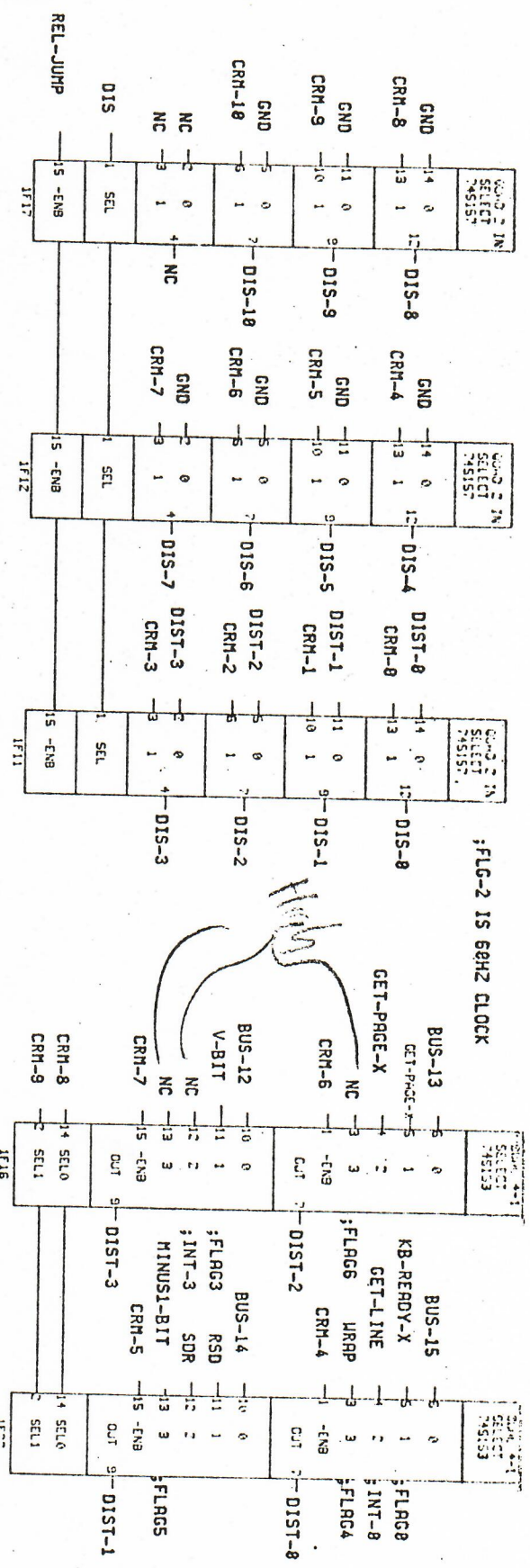
; LOGIC
0000 R 4000 ROTATE
0020 RB 4020 R - 1
0040 RB 4040 RDC
0060 NOR 4060 R+B
2000 OR 6000 R - B
2020 XOR 6020 SBC
2040 RROT 6040 R + 1
2060 ? 6060 RRS

; 7437'S REQUIRED TO DRIVE
LARGE ALU LOAD

C-BIT-L

C-BIT-LH

; MINUS-BIT is low if BUS-177777
; DISPATCH SELECTORS SHOULD BE S CHIPS
; DIS COMMAND SEL(2) MASK(4) 0000 MASK INVERTED
; RSD is UART data-out-ready
; SDR is UART-data-in-ready



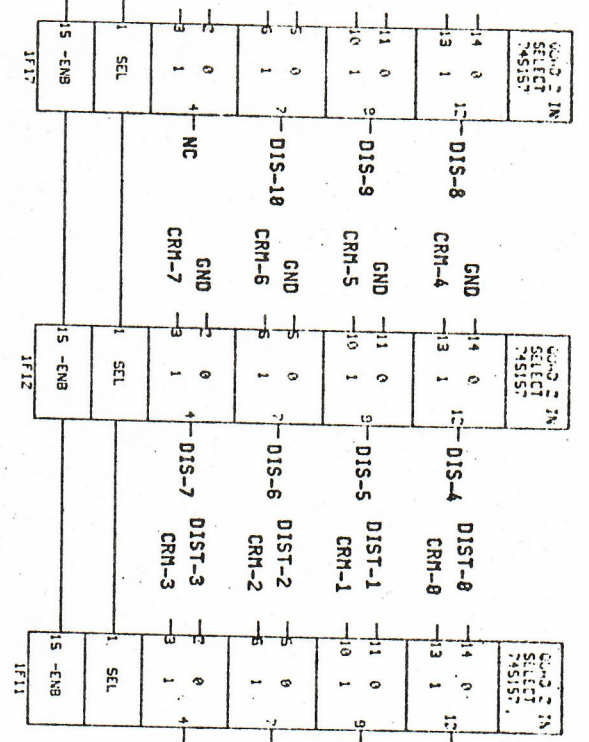
; FLAG-2 IS 60HZ CLOCK

GET-PAGE-X
CRN-6
CUT 3 -ENB
DIST-2

BUS-15
KB-READY-X
GET-LINE
INT-8
FLAG6
WRAP
CRN-4
CUT 3 -ENB
DIST-8

BUS-14
RSD
INT-3
SDR
MINUS-BIT
CRN-5
CUT 3 -ENB
DIST-1

BUS-12
V-BIT
NC
CRN-7
CUT 3 -ENB
DIST-3



COND IN
SELECT
745157

COND IN
SELECT
745157

COND IN
SELECT
745157

COND IN
SELECT
745153

COND IN
SELECT
745153

11000 A 0-2
1001 X 0-11
1010 X 0-5
1011 CPM 0-5

:B-INDIRECT HIGH CAUSES:
CPM-2 CPM-1 CPM-0

11100 A 0-2
1101 X 0-6:1110 X 0-2
1111 CPM 0-2

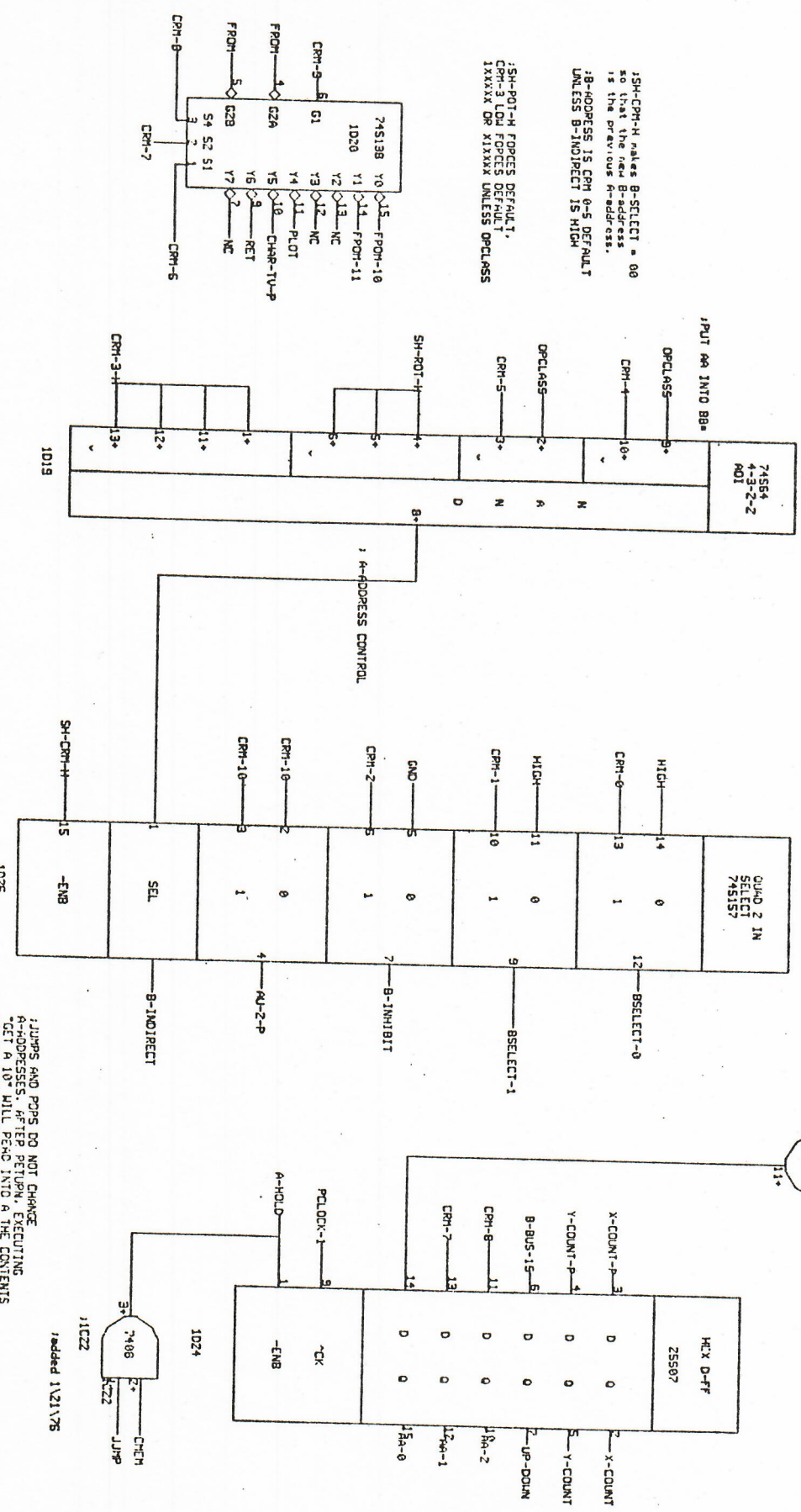
:SH-CPM-H makes B-SELECT = 00
so that the new B-address
is the previous A-address.
:B-ADDRESS IS CPM 0-5 DEFAULT
UNLESS B-INDIRECT IS HIGH
:SH-ROT-H FORCES DEFAULT.
CPM-3 LDA FORCES DEFAULT
1XXXXX OR XIXXXX UNLESS OPCLASS

ADDRESS CONTROL

MINSKY 2500

29-FEB-76 14:26

HQM: NTFH6



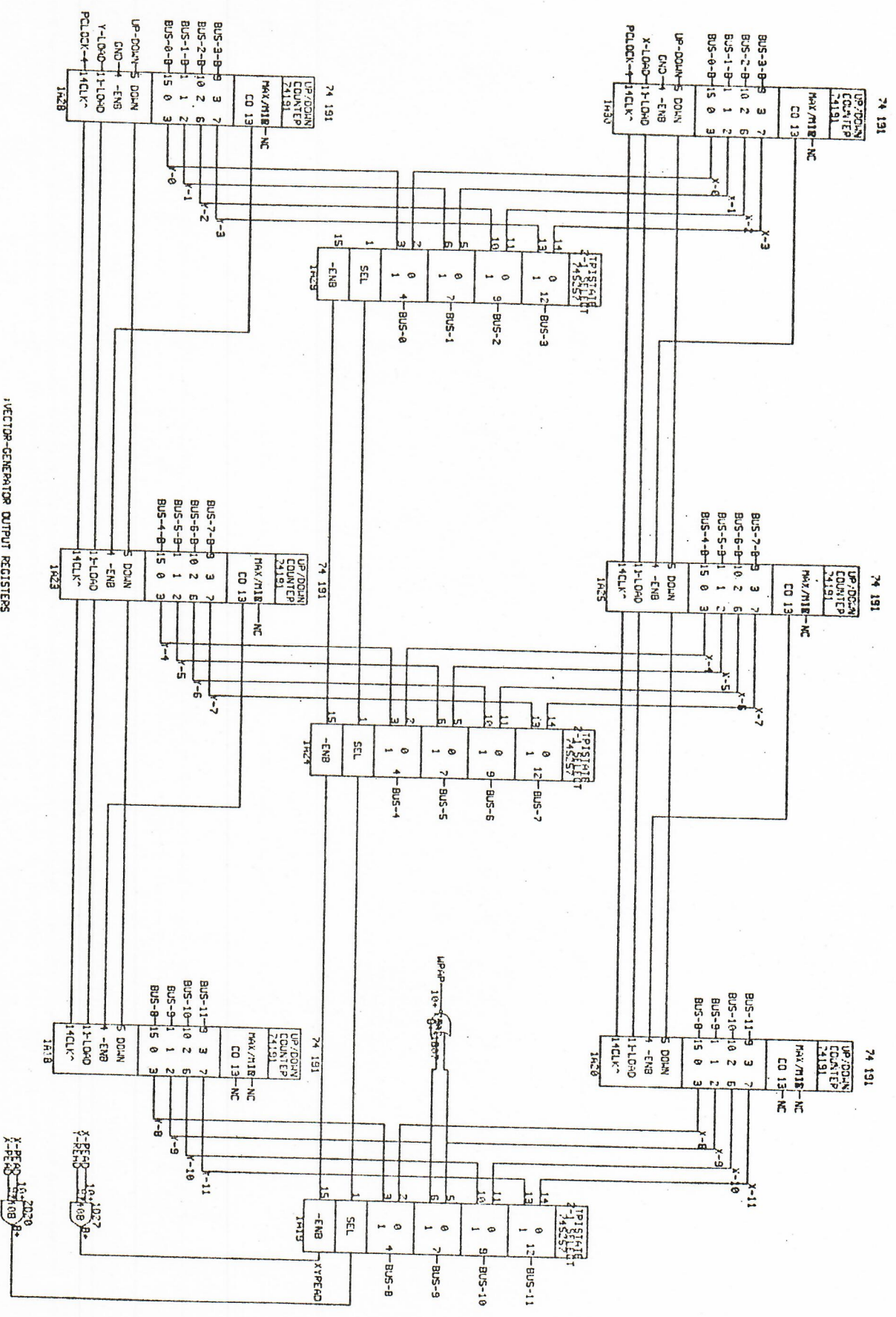
:JUMPS AND POPS DO NOT CHANGE
A-ADDRESSES. AFTER RETURN, EXECUTING
GET A 10* WILL SEND INTO A THE CONTENTS
OF THE LAST REGISTER LOADED

:Set M-0 = 0 on alternate
vector-generator cycles

added 1/21/76

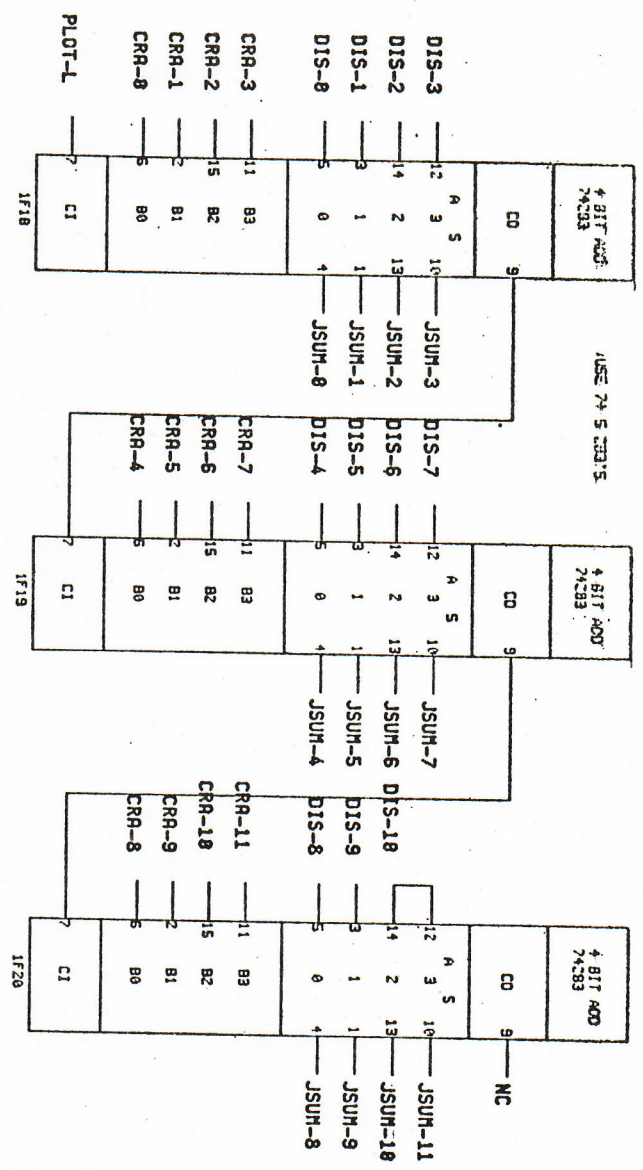


:CRM 0-5 DEFAULT



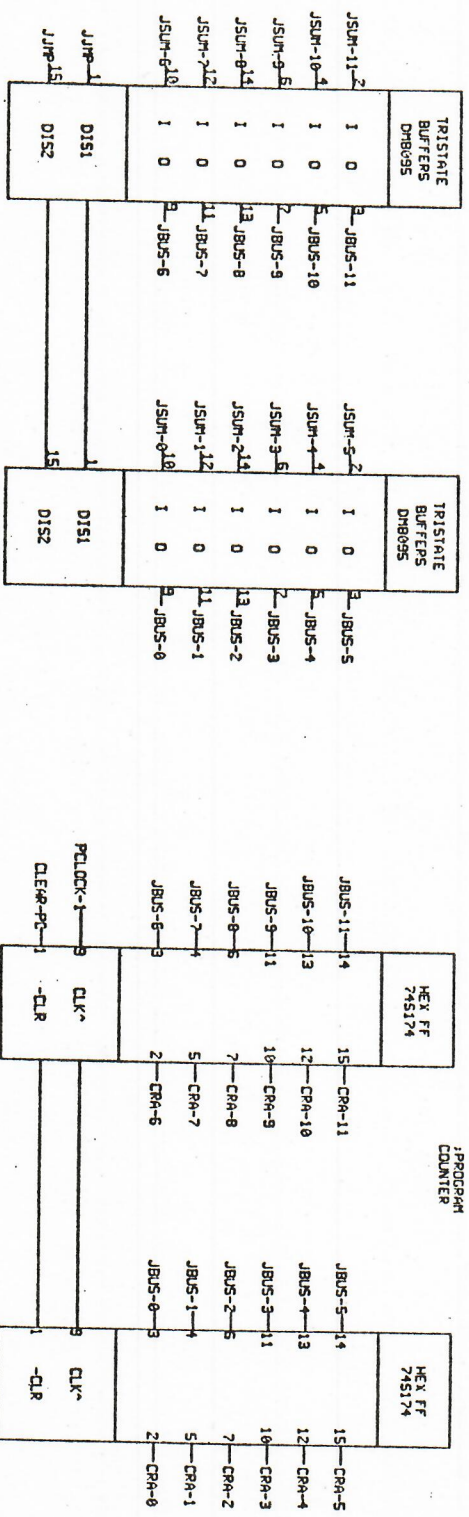
VECTOR GENERATOR OUTPUT REGISTERS

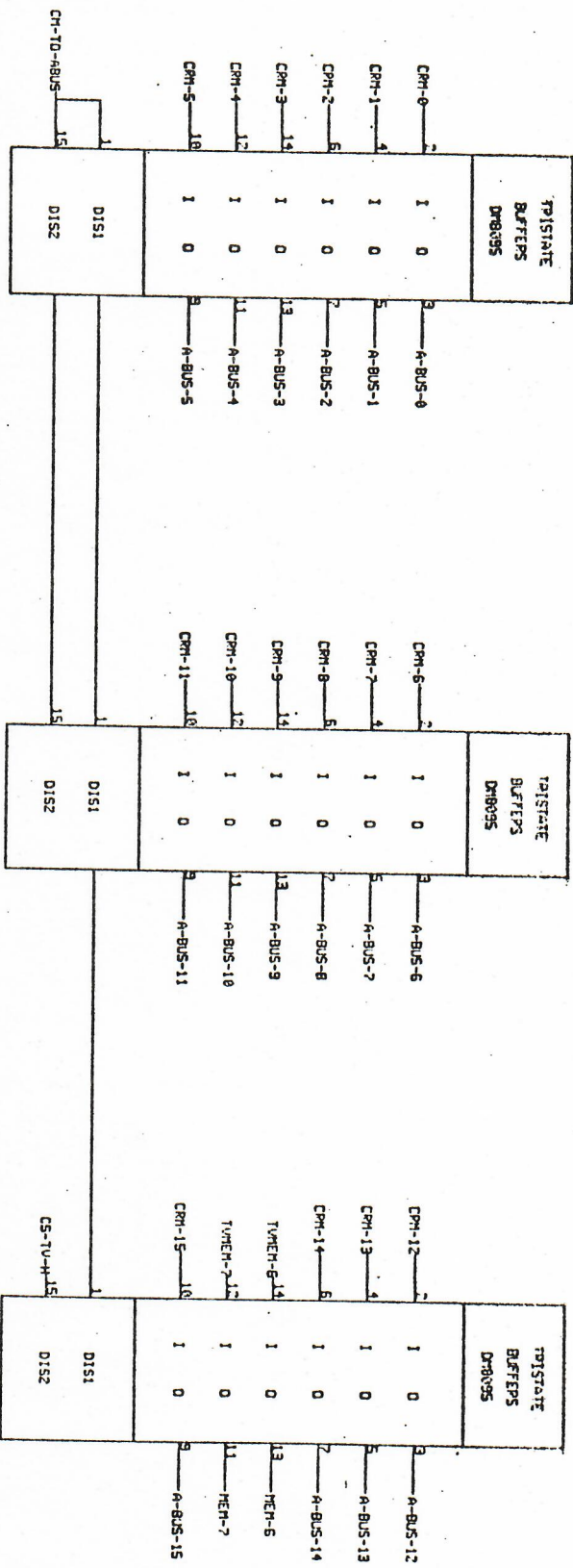
X-PEAD 10, 1027
X-PEB 10, 1027
BUFFER - DRIVEN FROM 7415130



1 BLOCKS ADD-1 DURING VECTOR

1 USE 73 367'S





IC12
THIS LINE PULLED LOW ENGAGES BOOTSTRAP LOADER

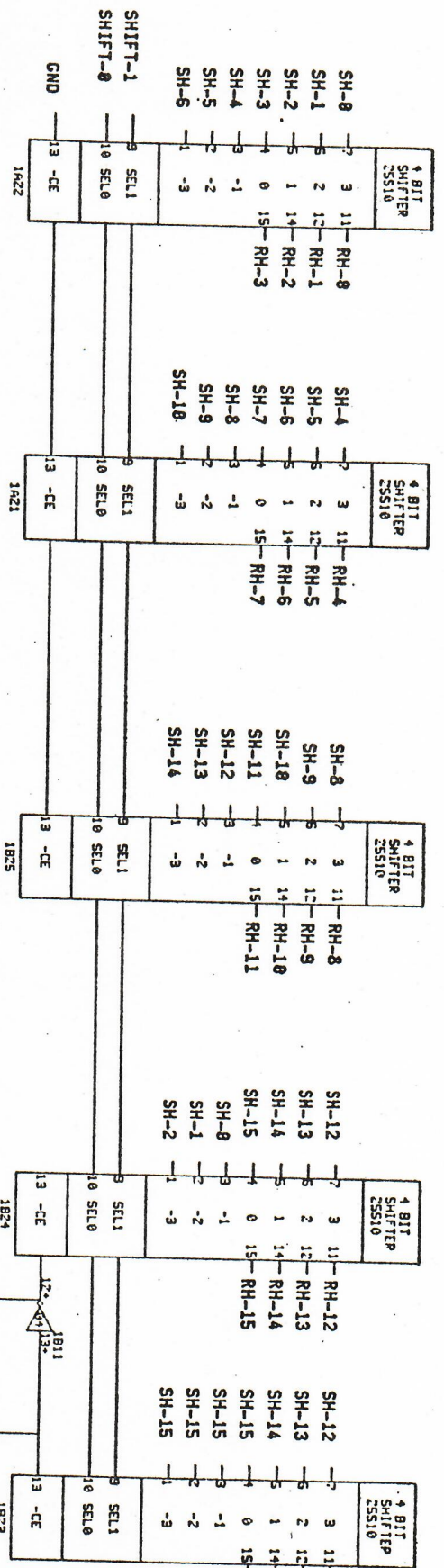
IC13
SEE NOTE-

IC14

When enabled, these gate CPM output into the A-BUS during the second phase of 32-bit instructions. The A-BUS lines on the register file are disabled and the INHIBIT lines prevent execution of the CPM data as an instruction.

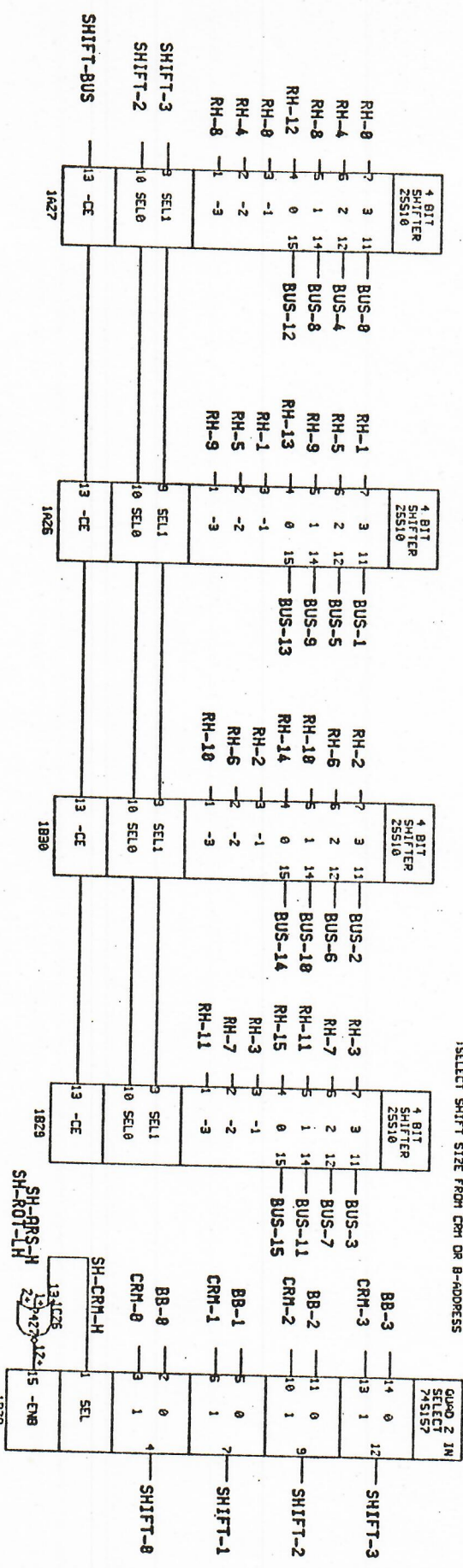
Bootstrap loader has to terminate with a jump and attach control memory. Next-to-last instruction should be DET (10) 23 to set un-load trigger. THE USE OF DET 10 1R IS ARBITRARY.

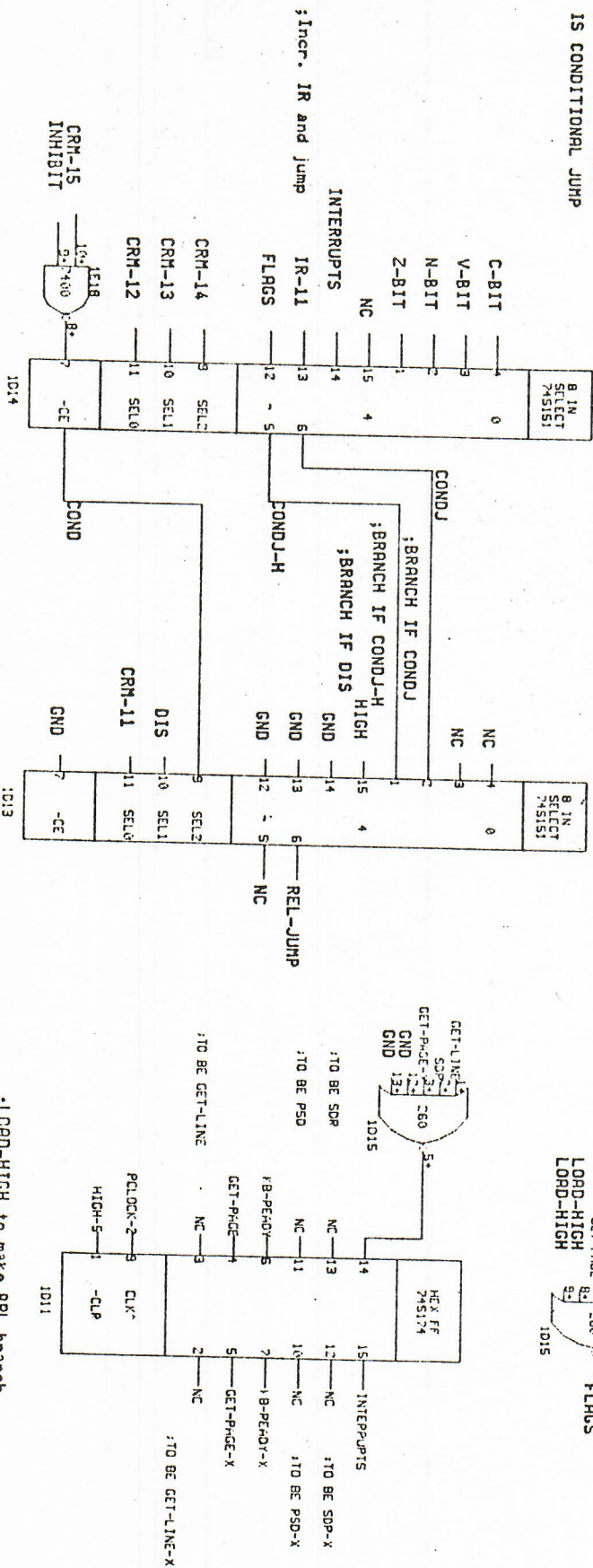
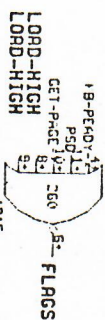
SHO
X131
X54A
13
XTE



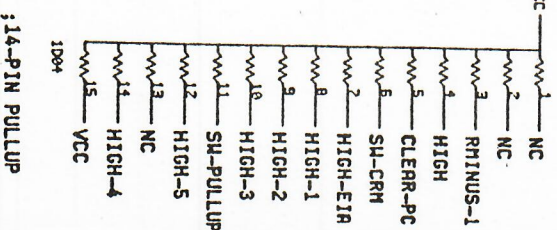
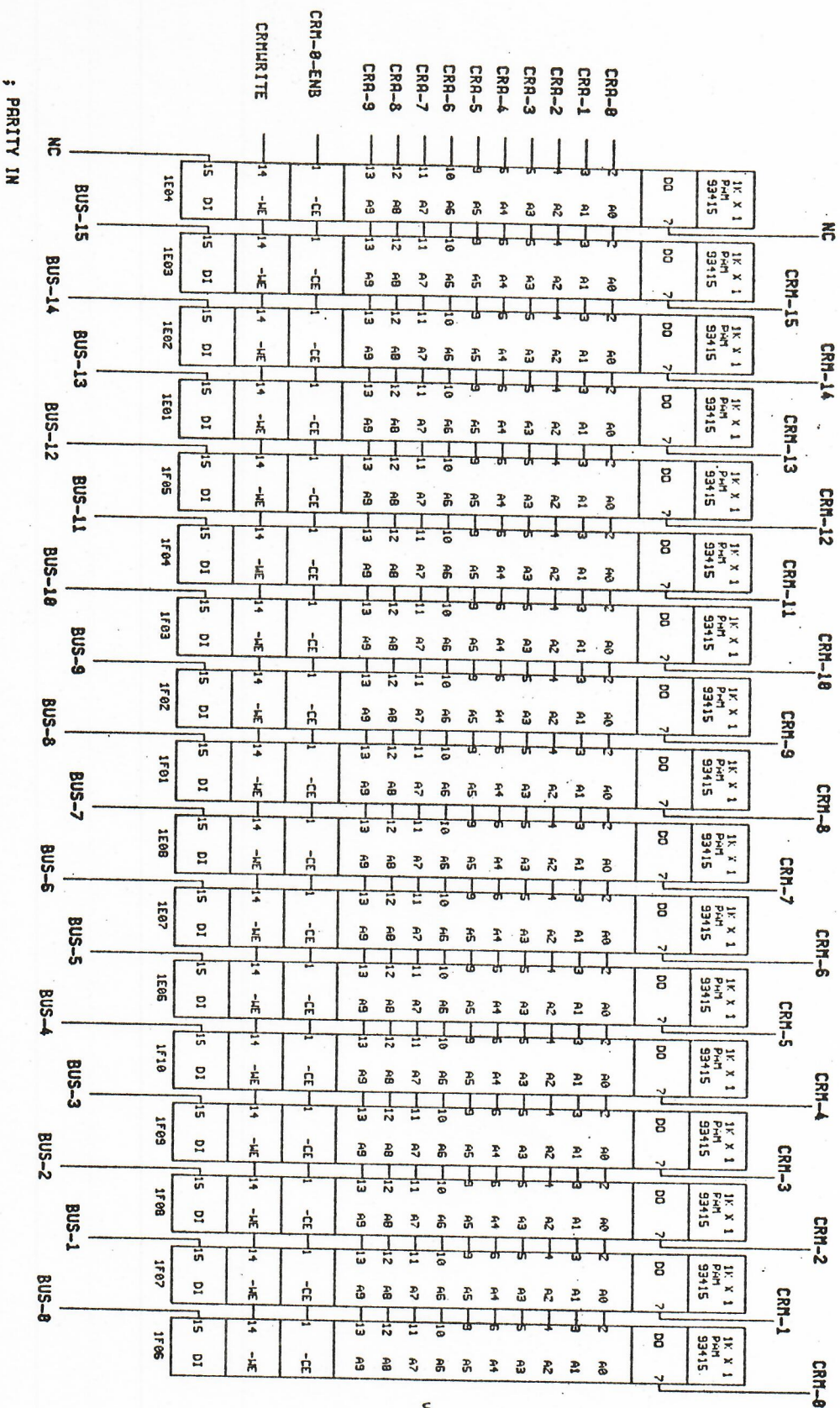
; ALU OUTPUT INTO "SH" INPUTS
 ; "RH" ARE INTERMEDIATE SHIFT LINES
 ; SHIFTER OUTPUTS GO TO MAIN BUS

; THREE STEPS OF ARITH RIGHT SHIFT
 ; SELECT SHIFT SIZE FROM CRM OR B-ADDRESS





;CRM-18 IS EXTRA BIT FOR PARITY OR WHATEVER



;USE 93425 TRI-STATE RAMS

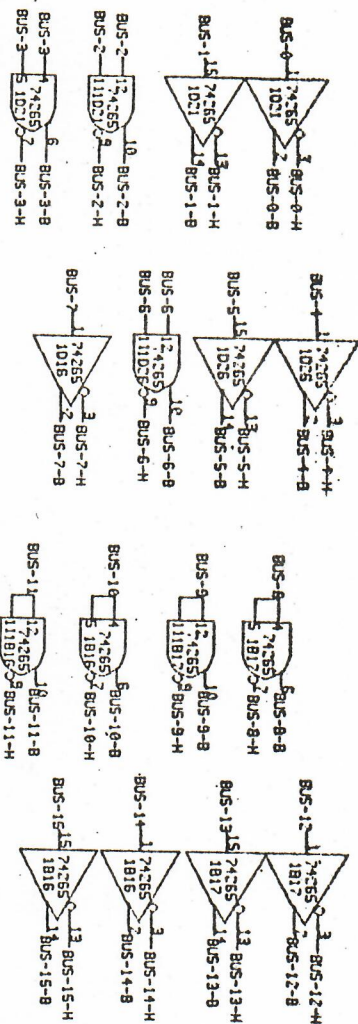
; PARITY IN

CONTROL MEMORY

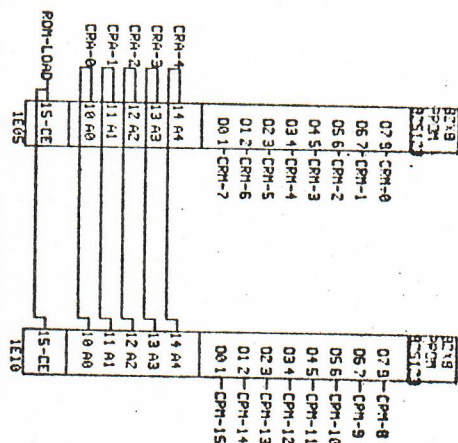
PULL-UPS

31-MAR-76 19:13

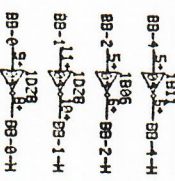
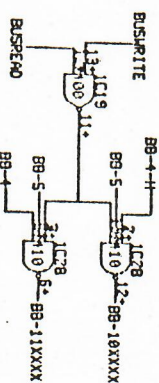
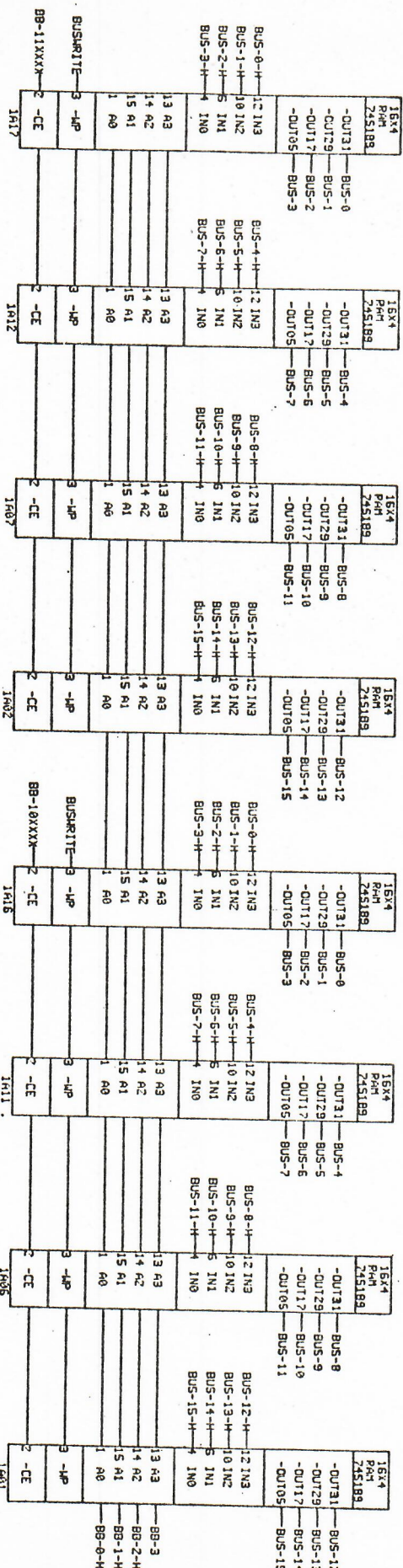
HQM: NTFH13

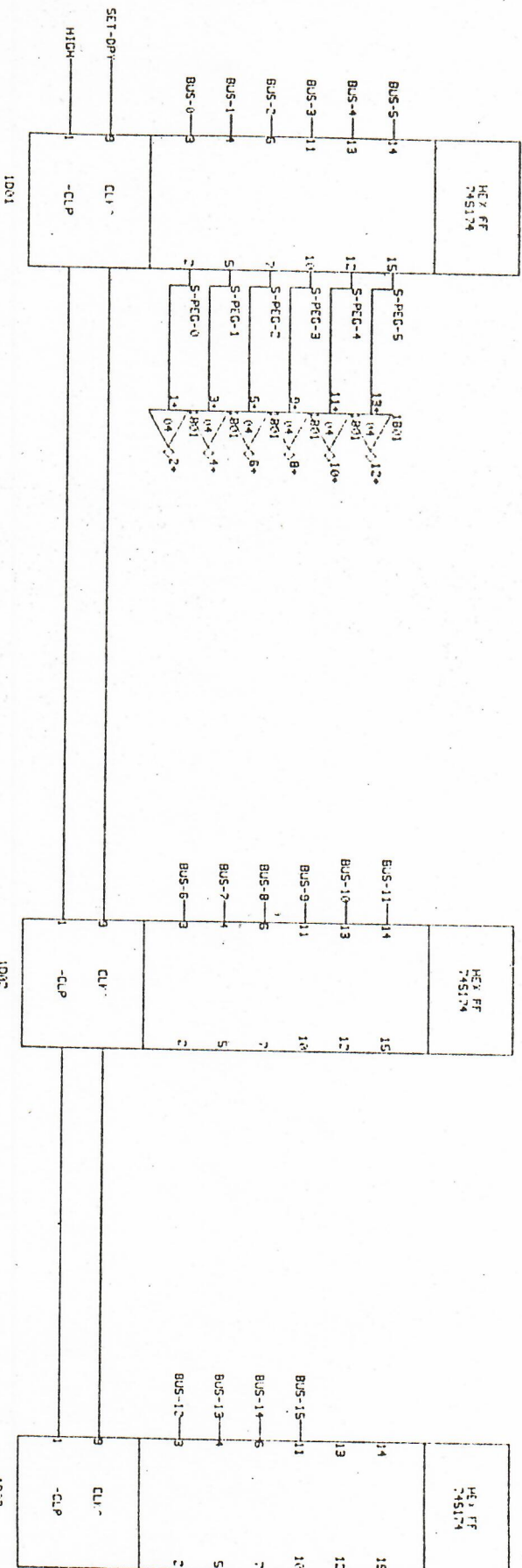


;BUS BUFFERED FOR GENERAL OUTPUT USE



;SOCKETS FOR TWO 32 X 8
ROWS FOR LOADER





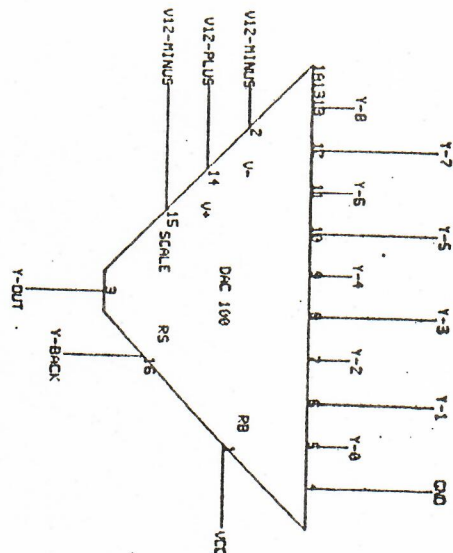
S-PEC-0 — RB1-0
 S-PEC-1 — RB1-1
 S-PEC-2 — RB1-2
 S-PEC-3 — RB1-3
 S-PEC-4 — RB1-4
 S-PEC-5 — RB1-5

NOTES

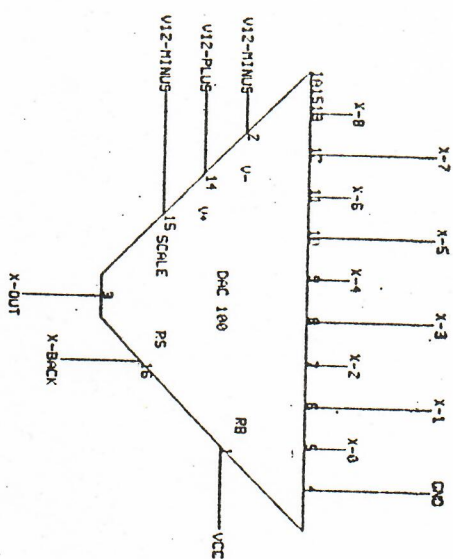
TFH ORDER CODE

04-APR-76 16:56

HQM: NTFH15

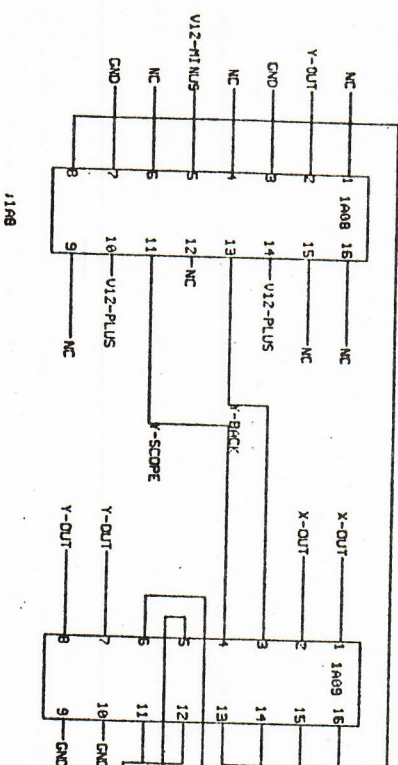


Y-OUT AND X-OUT NEED PROTECTION DIODES



THIS IS A 72247 DP-AMP

1A9



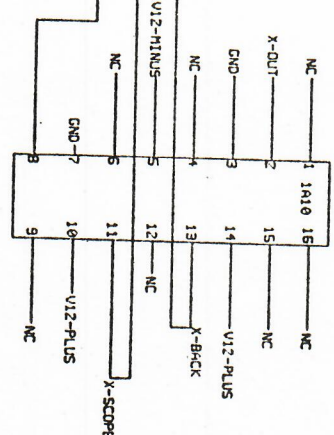
ANALOG FEEDBACK NET

PINS 4 AND 10 EACH HAVE 470PF CAP TO GND

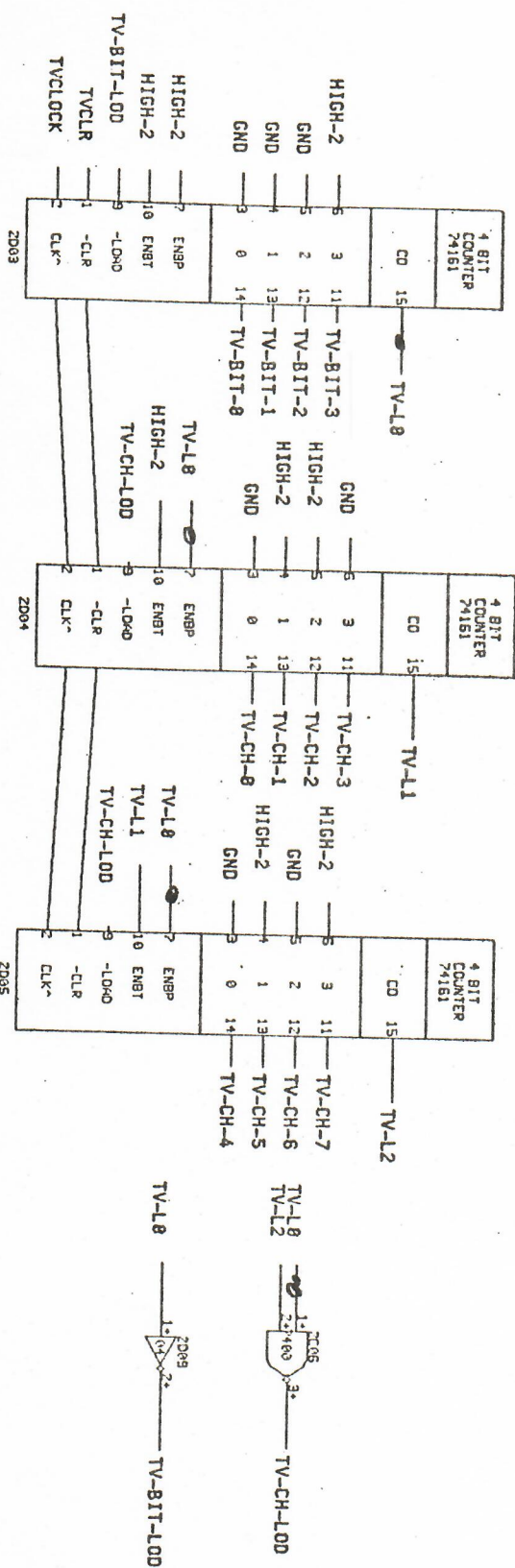
PINS 9 10 15 16 HAVE DMC PROTECTION DIODES

PUT NEAR VECTOR GENERATOR

- 1 - 914 DIODE - 16
- 2 - 914 DIODE + 15
- 1K RES
- 150K RES + 150PF CAP
- 3.3K RES + 150PF CAP
- 10K RES
- 7 - 914 DIODE + 10
- 8 - 914 DIODE - 9



1A10



NTFH18 COUNTER-CHAINS SHOULD NOT HAVE ANY CLEAR INPUT

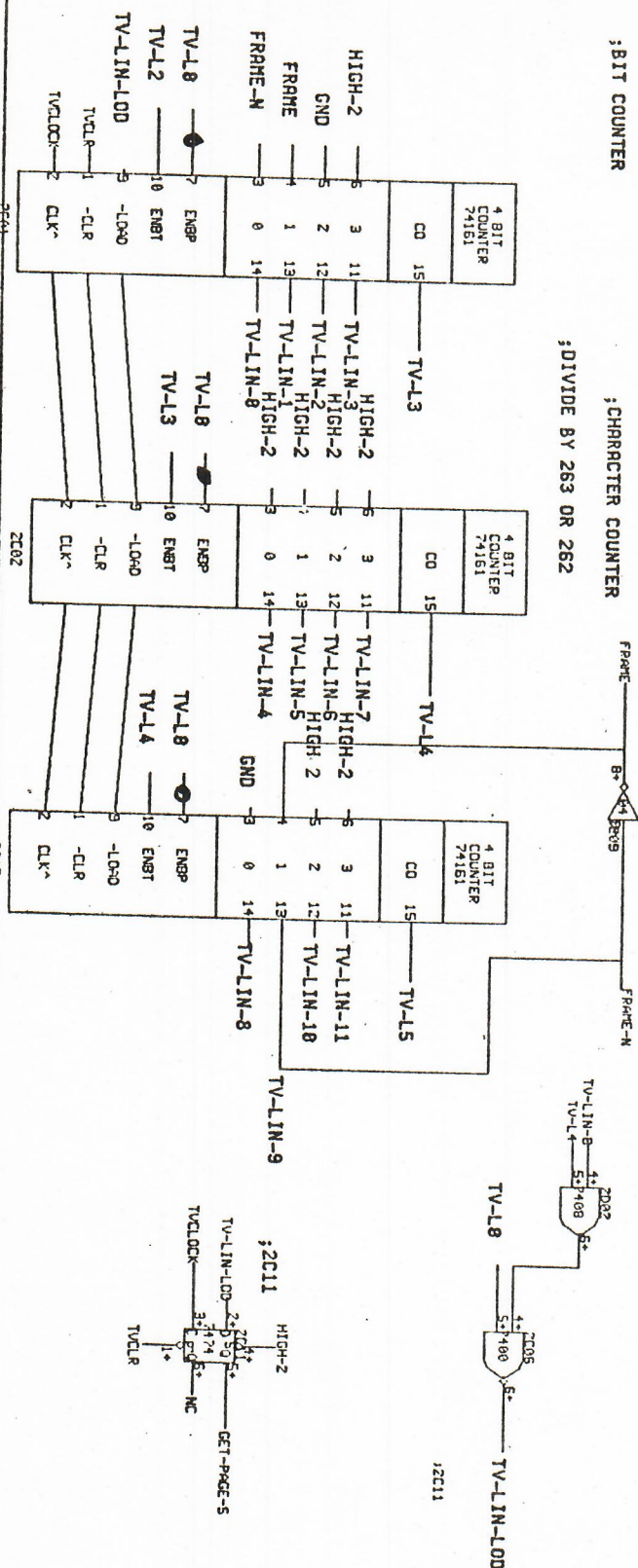
;DIVIDE BY 8

÷ DIVIDE BY 98

;BIT COUNTER

; CHARACTER COUNTER

;DIVIDE BY 263 OR 262



TIMING CHAIN

02-APR-76 15:14

HQM: NTFH 18

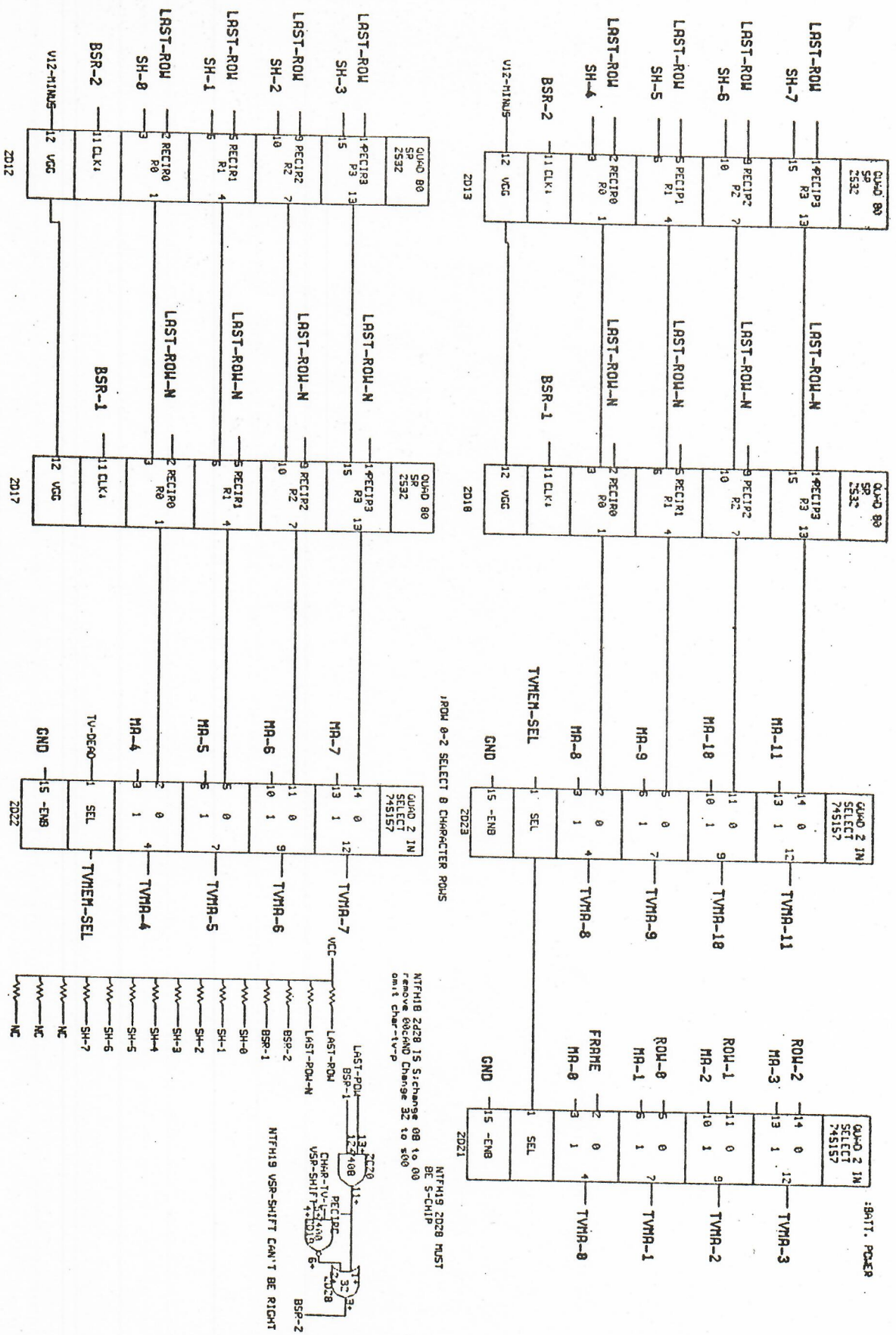
LINE BUFFERS

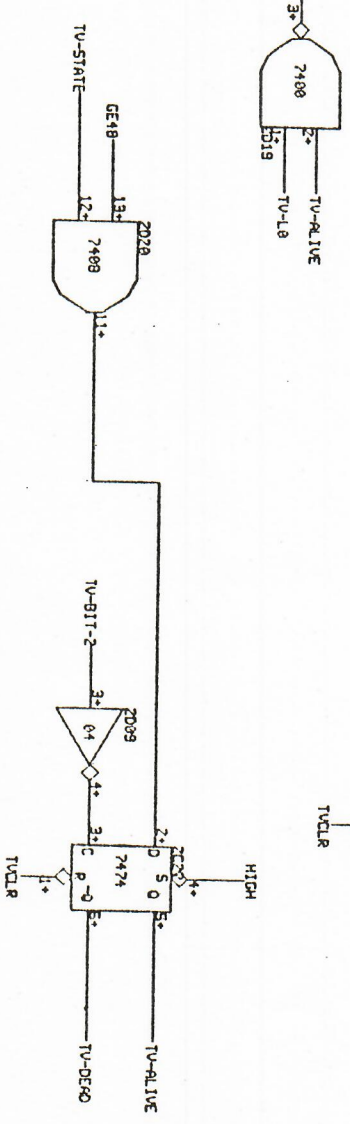
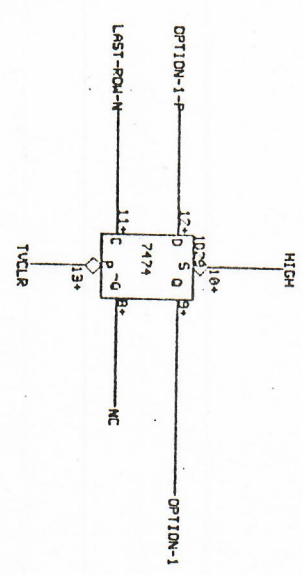
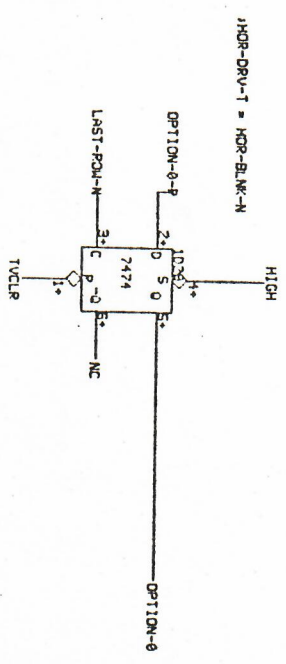
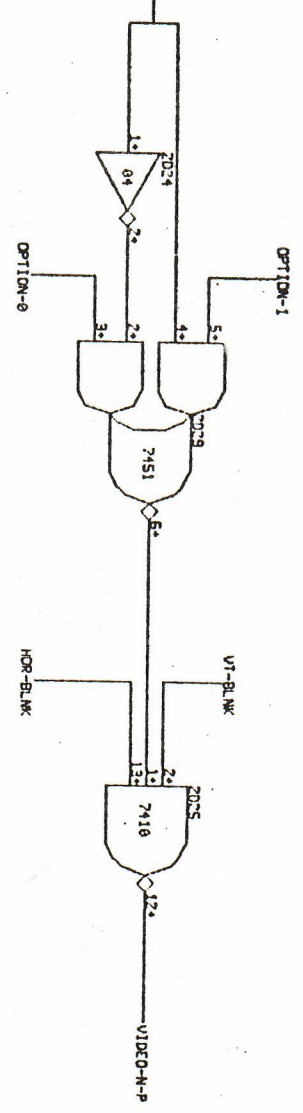
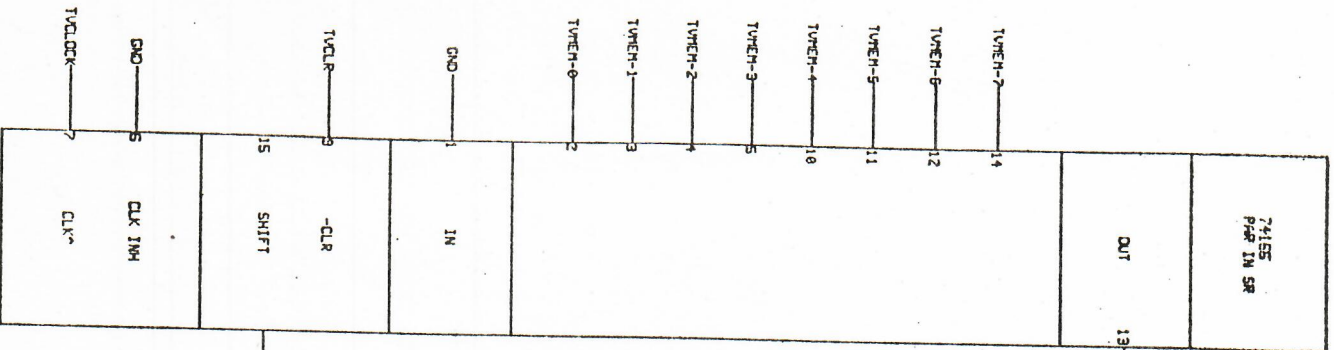
ADDRESS MULTIPLEXERS

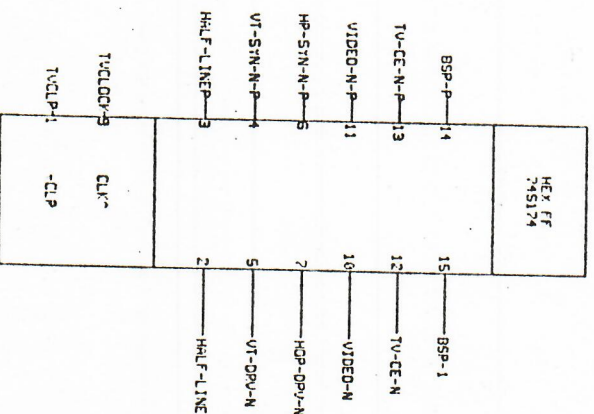
03-APR-76 18:11

HQM: NTFH19

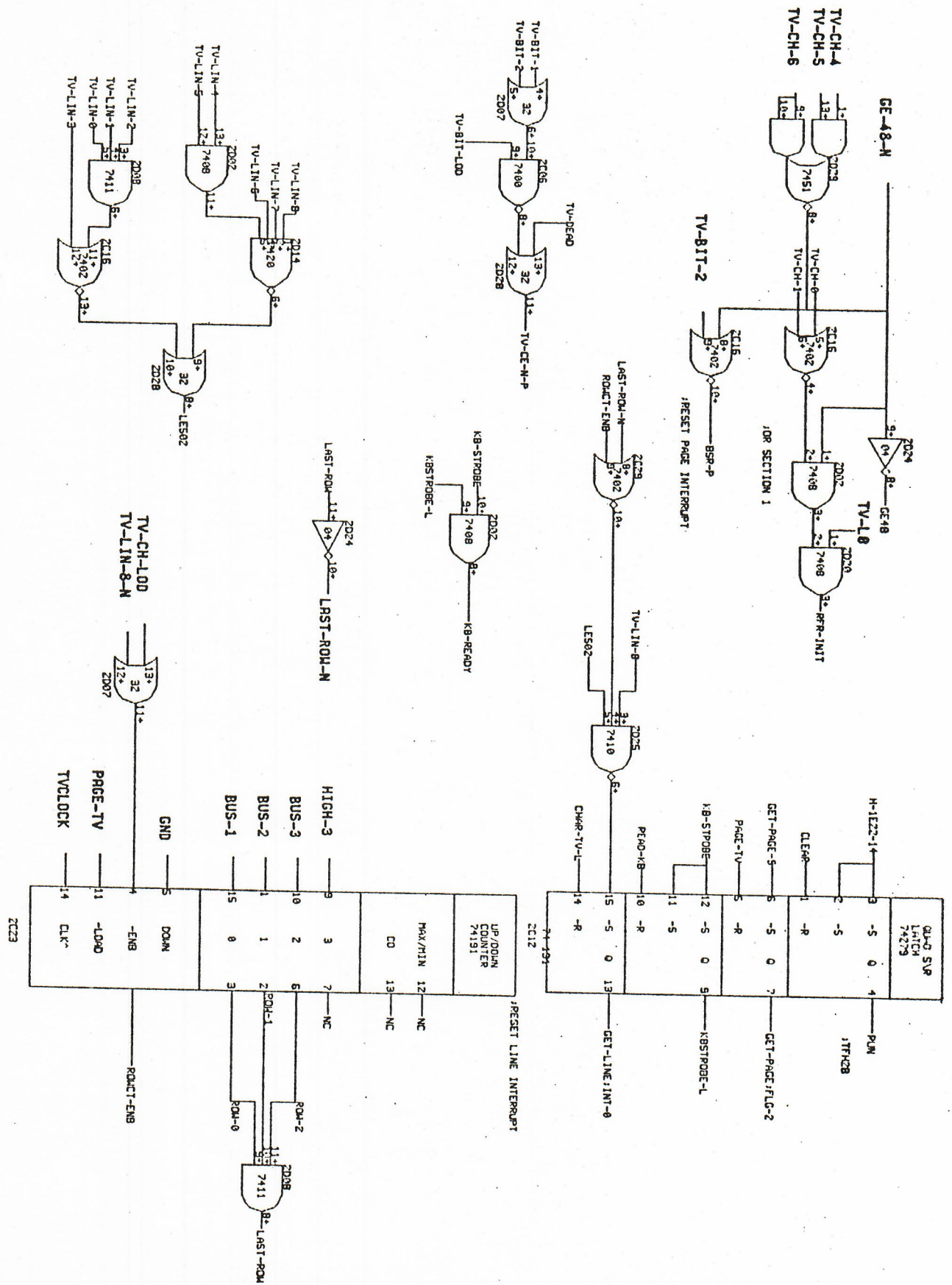
RECIRCULATE TEXT-LINE TEXT-19: 2024 1292402023 MUST BE LS 157 CHIPS

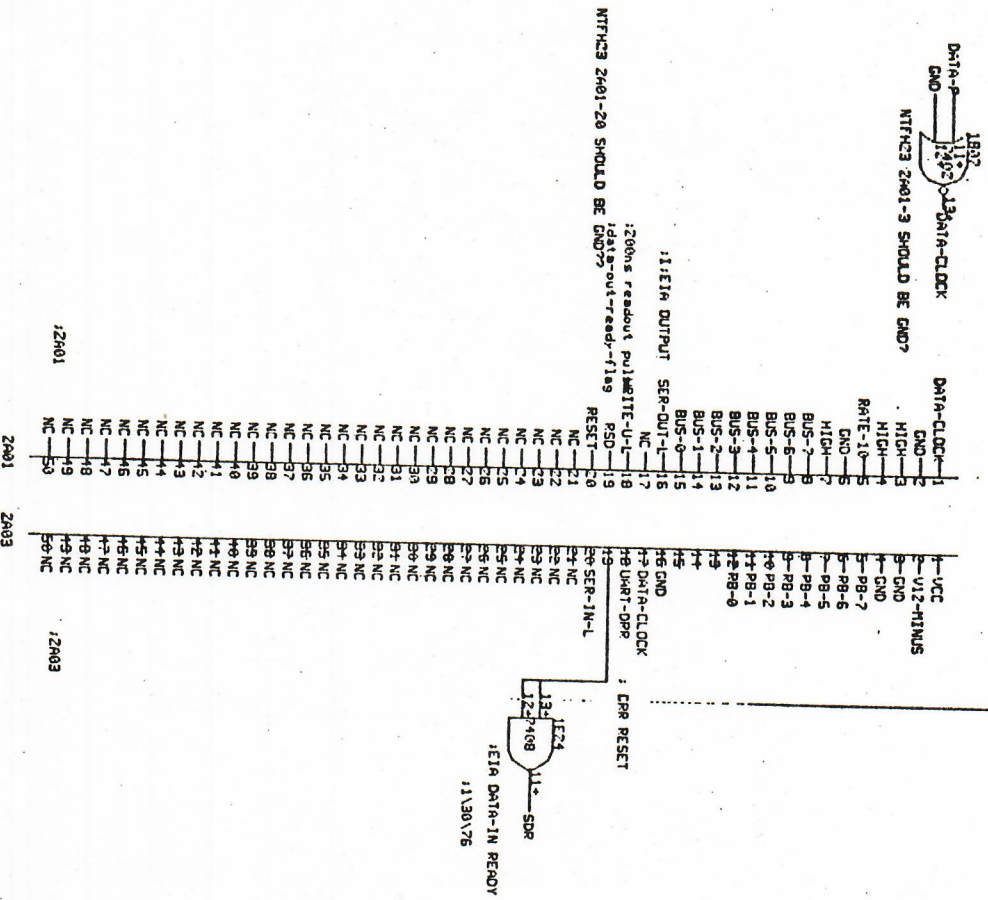


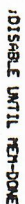




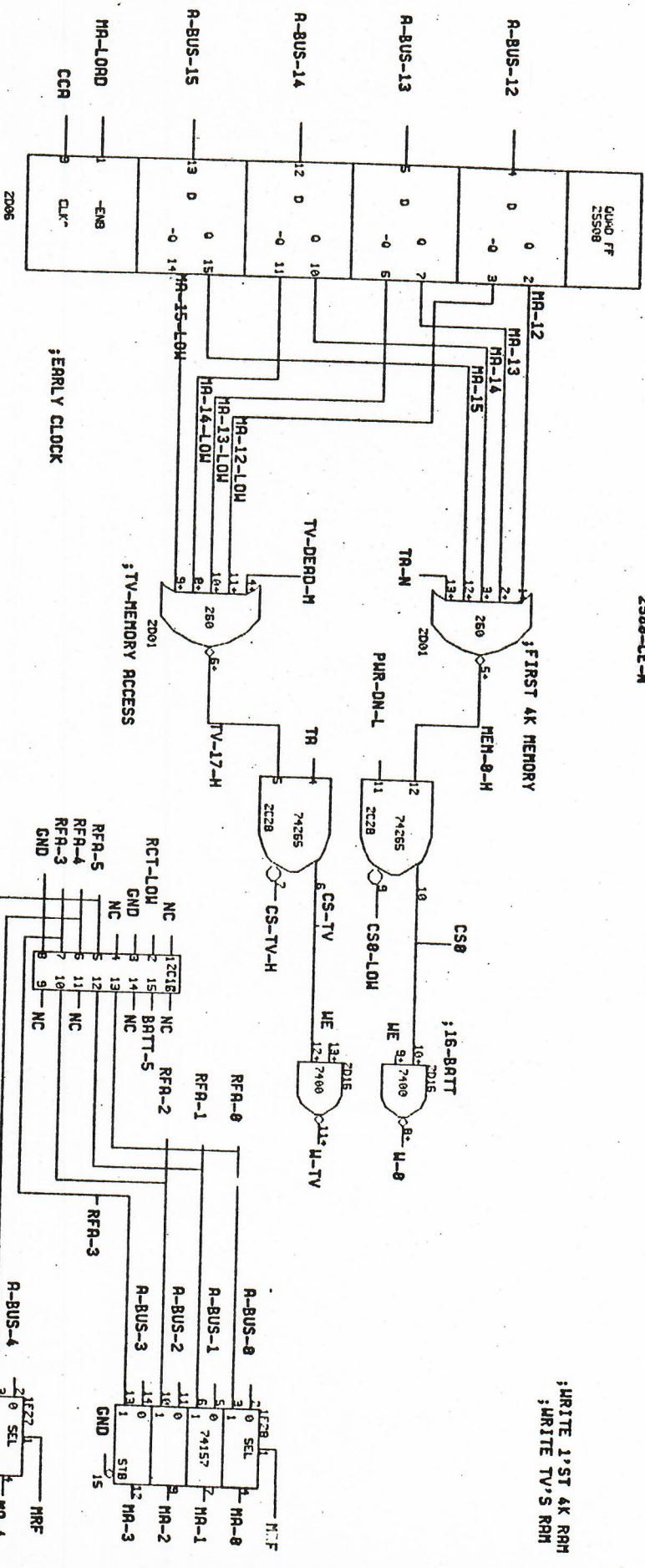
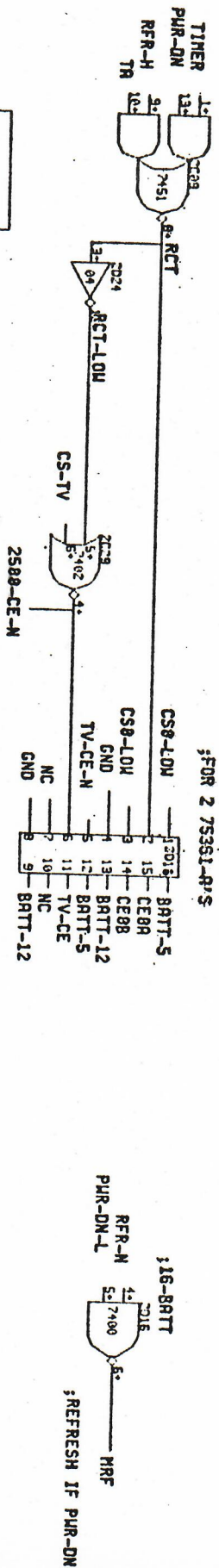
:2622 PLUS







HQM: NTFH24



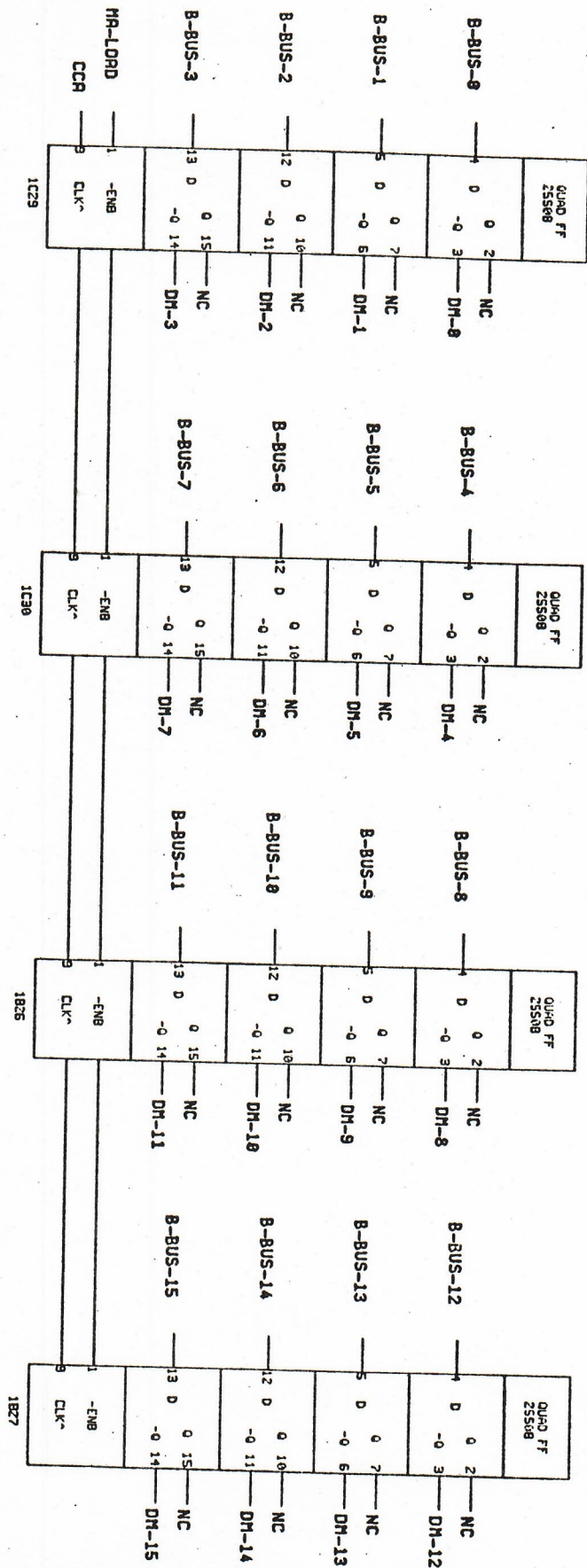
MR-LORD CIRCUITS?

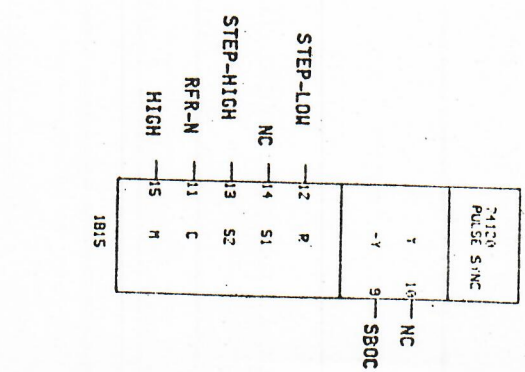
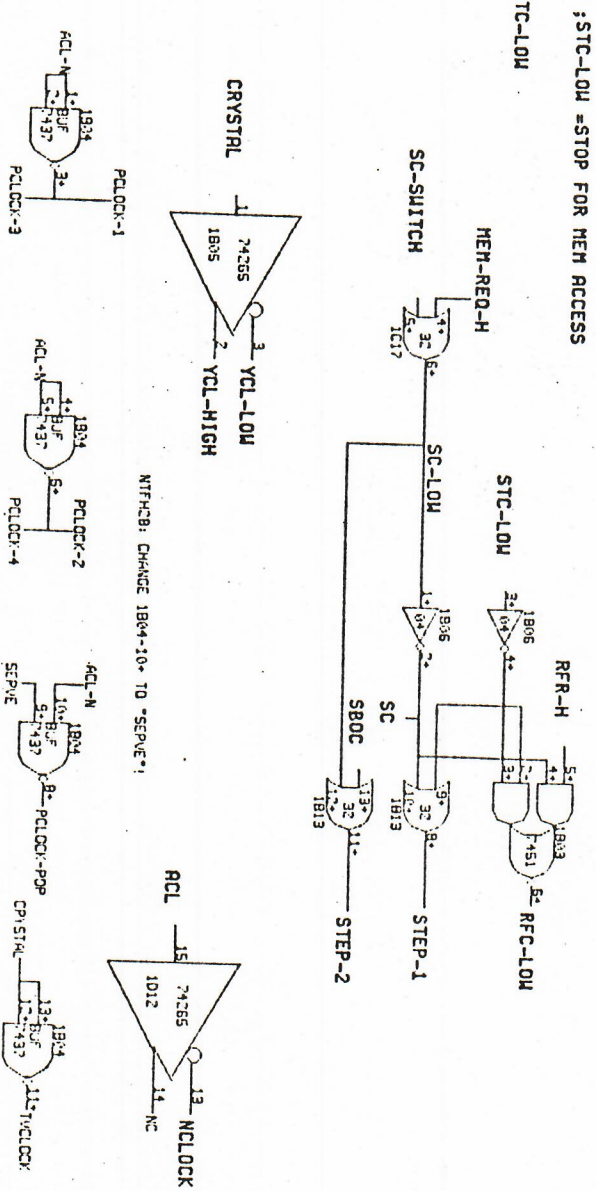
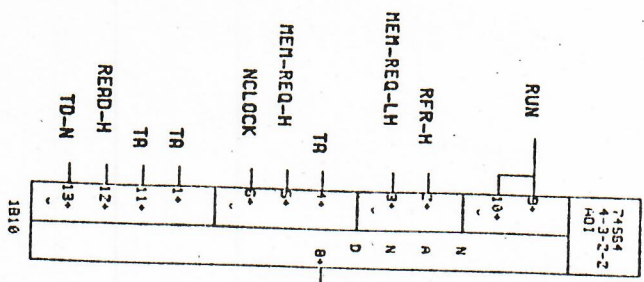
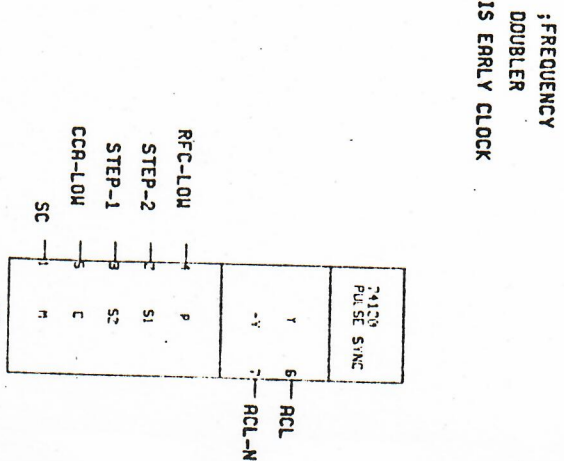
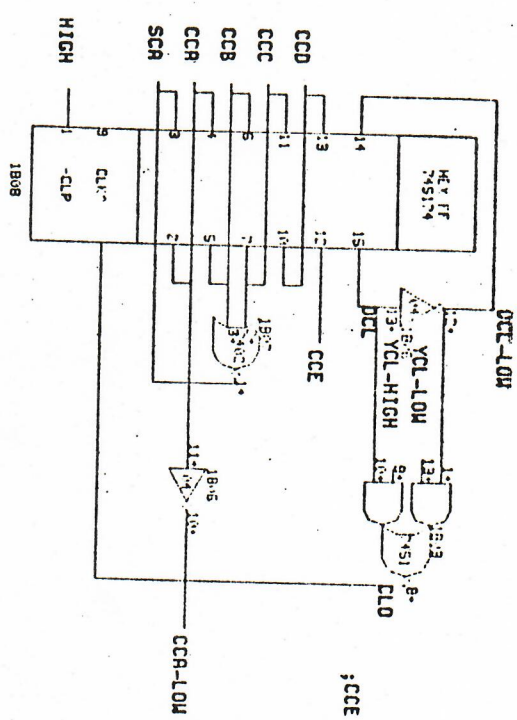
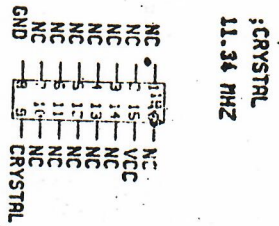
2C17
4824 CMOS 7-BIT CTR

16-BATT

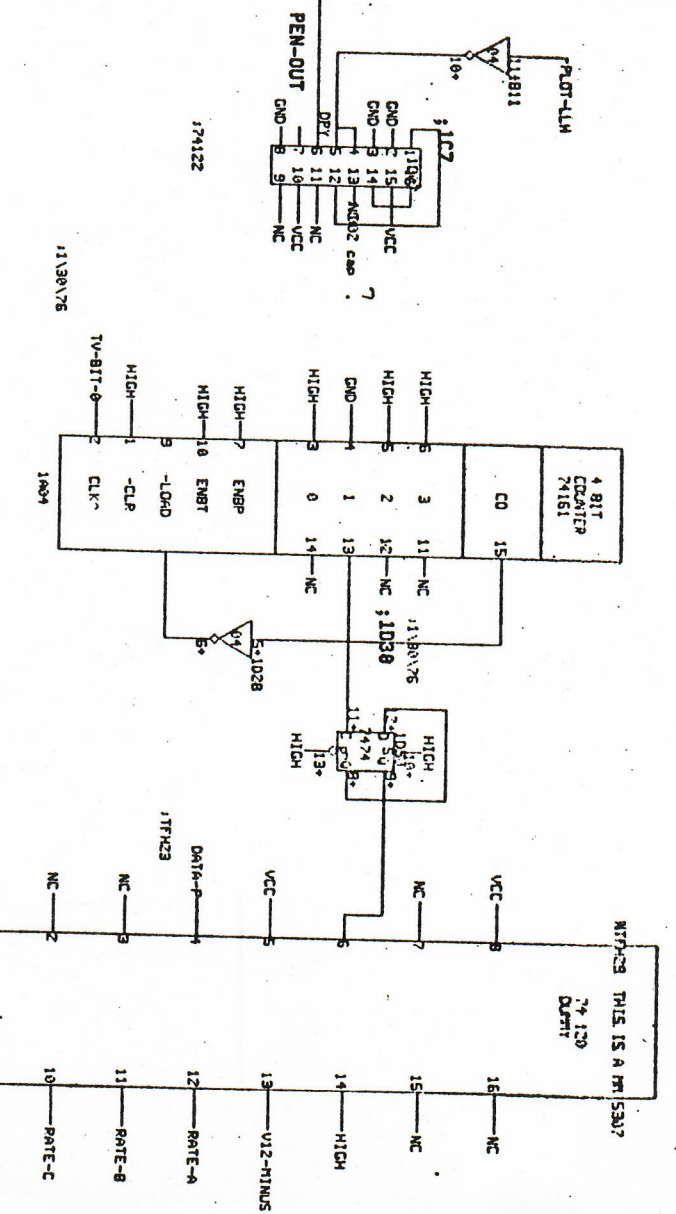
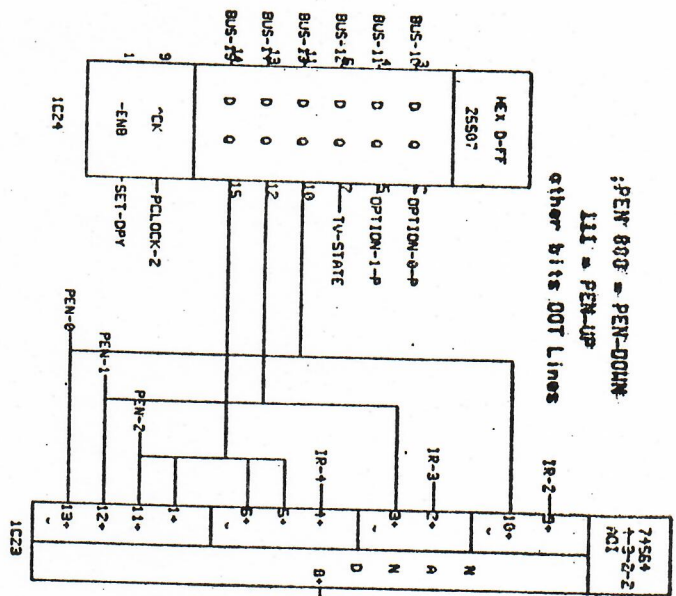
HQM: NTFH26



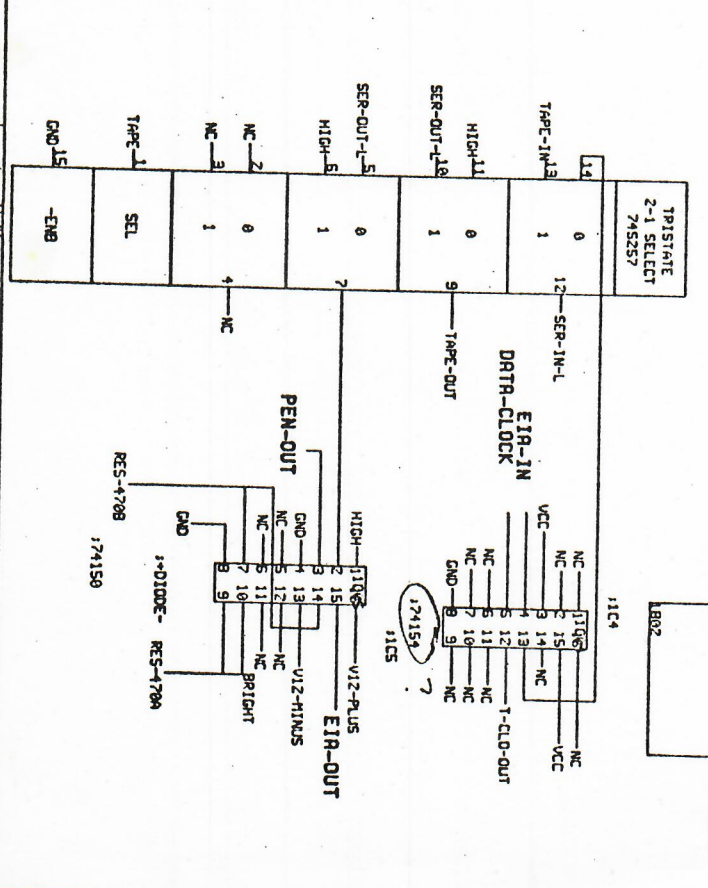
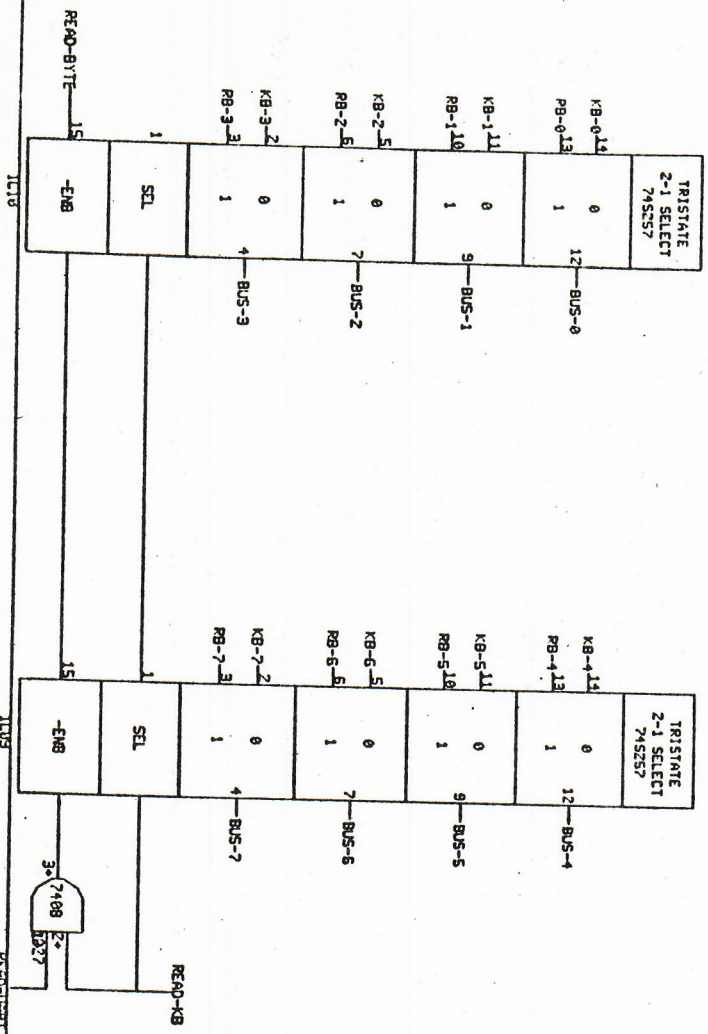




:PEN 800 = PEN-DOWN
 111 = PEN-UP
 other bits OUT Lines



DATA RATE SELECTOR



31-MAR-76 16:27

HQM: NTFH29

